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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/368,918	08/05/1999	RICHARD L. TRABER	3COM-2200.IP	6088

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/368,918	TRABER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 August 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on August 19, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Response to Amendment

2. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner would like to point out that the Applicant teaches that a trigger signal is applied to a first stage and captured at subsequent stages as it pass through the

multiple stages. The Examiner would like to point out that the Applicant attempts to use the phrase "a trigger signal captured during multiple stages" to capture the Applicant's teachings. The definition of during (throughout the duration of or at a point in the course of a time period) requires that during be followed by an instant of a time period or a time period and multiple stages is neither an instant of a time period or a time period hence "a trigger signal captured during multiple stages" is ambiguous and fails to enable a reasonable interpretation without undue and excessive experimentation or analysis. The Examiner assumes "a trigger signal captured at multiple stages as the signal passes through the multiple stages" was meant (which is clearly the Applicnt's intent since that is the only embodiment that the Applicant teaches, see the Applicant's Figure 1).

Claims 9-10 depend from claim 1, hence inherit the deficiencies of claim 1.

4. Claims 1-10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "during multiple stages" in claim 1 is used by the claim to mean "at multiple stages as the signal passes through the multiple stages ", while the term is grammatically incorrect.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 3 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Li, Hehching Harry (US 6023778 A).

6. Li anticipates claim 1.

Li teaches an automatic scan test enable signal assertion system (see Figures 3 & 4B; col. 3, lines 55-67 and col. 4, lines 21-31, Li) comprising: a scan test enable trigger sensing component (see OR circuit 94, Li) adapted to provide an assertion or deassertion notification when logical values of a trigger signal (scan mode signals received via mode input 53 are trigger signals, col. 3, lines 59-58, Li) captured during multiple stages (see 97, 98 and 100 in Figure 4B, Li) provide an indication to begin a

scan test enable signal assertion or deassertion (see 55 in Figure 4B and col. 4, lines 1-2, Li; Note: mode output makes available the scan mode signal to the Mux Scan Flip-Flops to enable the scan test); and a staging component (see 91 in Figure 4B, Li) coupled to said scan test enable trigger sensing component (see OR circuit 94, Li), said staging component adapted to advance said logical values of said trigger signal through a plurality of stages in accordance with a progression signal (clock signal 52, in Figures 3 & 4B in Li, is a progression signal) and issue an asserted or deasserted scan test enable signal based upon said assertion or deassertion notification from said scan test enable trigger sensing component (see Abstract, Li).

7. Li anticipates claim 3.

Figure 3 is an embodiment of a test circuit (col. 3, lines 55-60, Li).

8. Li anticipates claim 15.

Li teaches automatic scan test enable signal assertion method (see Figures 3 & 4B; col. 3, lines 55-67 and col. 4, lines 21-31, Li) comprising the steps of:

a) transitioning logical values of a trigger signal (see 202 in Figure 5, Li);

b) asserting a scan test enable signal (see 204 in Figure 5, Li) based upon logical values in said trigger signal (see 202 & 203 in Figure 5, Li);

c) suspending transitions in a stage progression signal (see 201 & 207 in Figure 5, Li);

d) deasserting said scan test enable signal if a transition occurs in said stage progression signal (see 213 in Figure 5, Li); and

e) utilizing a normal functional pin to communicate said trigger signal and said stage progression signal (see 250 and 51 in Figure 3, Li).

9. Li anticipates claim 16.

See 211 in Figure 5, Li.

10. Li anticipates claim 17.

See 201 and 205 in Figure 5, Li.

11. Li anticipates claim 18.

See 98 and 100 in Figure 4B, Li.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 2, 4-14 and 19-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Hehching Harry (US 6023778 A).

13. 35 U.S.C. 103(a) rejection of claim 2.

Li substantially teaches the claimed invention described in claim 1 (as rejected above). However Li does not explicitly teach the specific use of a PCI reset signal as a trigger signal.

The Examiner would like to point out that a reset signal is a binary signal as expected from the scan mode pad 50 in Figure 3, hence use of a reset signal does not deviate from the scope or the intent of the teachings in Li, since a reset signal is a binary signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li by including use of a PCI reset signal as a trigger signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a PCI reset signal as a trigger signal would have provided a a binary means as taught in the Lee patent for enabling the test.

14. Li teaches the additional limitations of claims 4 and 7.

The Examiner would like to point out that the Li teaches two stages to delay the test enable signal. Expanding to a specific embodiment with a means for delaying the test enable signal with three stages does not deviate from the scope or the intent of the

teachings in Li, since one of ordinary skill in the art at the time the invention was made would have known that a third stage would add an additional clock delay. The Examiner would also like to point out that given the clocking requirements of Figure 5 in Li, one of ordinary skill in the art at the time the invention was made would have known how to design a circuit to implement the requirements. One ordinary skill in the art at the time the invention was made would also have known how to implement an embodiment with a three-cycle clock delay.

15. Li teaches the additional limitations of claim 5.

See Rejection to claim 2, above.

16. Li teaches the additional limitations of claim 6.

See 201 and 204 in Figure 5, Li.

17. Li teaches the additional limitations of claims 8 and 9.

See Rejection to claim 5 and Figure 5 in Li.

18. Li teaches the additional limitations of claim 10.

A particular embodiment for the test activation system does not deviate from the scope or the teachings of the Li patent (see rejections to claims 1-9, above).

19. 35 U.S.C. 103(a) rejection of claim 11.

Li teaches an automatic scan test enable signal activation system comprising: a scan test enable signal assertion system (see Figures 3 & 4B; col. 3, lines 55-67 and col. 4, lines 21-31, Li) adapted to automatically assert or deassert the scan test enable signal in response to transitions in a trigger signal and stage progression signal (scan mode signals received via mode input 53 are trigger signals, col. 3, lines 59-58, Li; and clock signal 52, in Figures 3 & 4B in Li, is a progression signal); a mutliplexer (MUX) coupled to said automatic scan test enable signal assertion system (see MUX's 62, 68, 75, 81 and 87 in Figure 3 in Li), said multiplexer is adapted to facilitate transmission of signals depending upon the assertion of a scan test enable signal (see delay Circuit 54 and MUX's 62, 68, 75, 81 and 87 in Figure 3 in Li); a functional component coupled to said multiplexer (see Integrated Circuit Logic 70 in figure 3 of Li), said functional component is adapted to perform normal operations of an ASIC or printed circuit board (col. 1, lines 9-11, Li); an input port coupled to said functional component (see 72 in Figure 3, Li), said input port is adapted to function as input connections that communicate signals to said ASIC or said printed circuit board; an MUX Scan Flop 75 gate coupled to said input port, said MUX Scan Flop 72 gate is adapted to capture information from said input port; and a test data output port (see 72 in Figure 3, Li) coupled to said multiplexer, said test data output port adapted to communicate test data off of the Integrated Circuit 70 (see 76 in Figure 3, Li).

However Li does not explicitly teach the specific use of a NAND gate coupled to said input port.

The Examiner would like to point out that the NAND gate serves the purpose of capturing data to be inputted into a functional logic component of an integrated circuit. The MUX's 62 and 68 in LI serve the purpose of capturing data to be inputted into a functional logic component of an integrated circuit hence using a NAND gate in place of the MUX in Fig. 3 of Li does not deviate from the scope or the intent of the teachings in the Li patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li by including use of a NAND gate coupled to said input port. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a NAND gate coupled to said input port would have provided a means for capturing data to be inputted into a functional logic component of an integrated circuit.

20. Li teaches the additional limitations of claim 12.

The MUX's 62 and 68 in LI serve the purpose of capturing data to be inputted into a functional logic component of an integrated circuit hence using a NAND gate in place of the MUX in Fig. 3 of Li does not deviate from the scope or the intent of the teachings in the Li patent.

21. Li teaches the additional limitations of claim 13.

See Figure 3 in Li and rejections to claims 11 and 12, above.

22. Li teaches the additional limitations of claim 14.

See MUX F-F 75 in Figure 3 of Li.

23. 35 U.S.C. 103(a) rejection of claim 19.

Li substantially teaches the claimed invention described in claims 15-18 (as rejected above).

However Li does not explicitly teach the specific use of asserting said trigger signal if it is at a logical 1 value during a first stage and the trigger signal is at a logical 0 value during a second stage and third stage.

The Examiner would like to point out that the Li teaches two stages to delay the test enable signal. Expanding to a specific embodiment with a means for delaying the test enable signal with three stages does not deviate from the scope or the intent of the teachings in Li, since one of ordinary skill in the art at the time the invention was made would have known that a third stage would add an additional clock delay. The Examiner would also like to point out that given the clocking requirements of Figure 5 in Li, one of ordinary skill in the art at the time the invention was made would have known how to design a circuit to implement the requirements. One ordinary skill in the art at the time the invention was made would also have known how to implement an embodiment with a three-cycle clock delay.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li by including use of asserting said trigger signal if it is at

a logical 1 value during a first stage and the trigger signal is at a logical 0 value during a second stage and third stage. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a specific embodiment with three stages for test assertion would have provided a means for delaying the test enable signal for three clock signals.

24. Li teaches the additional limitations of claim 20.

See rejection to claim 2, above.

25. Li teaches the additional limitations of claim 21.

See rejection to claim 1, above and Figures 4B and 5 in Li.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Graef, Stefan (US 5831993 A) teaches a scan chain in a semiconductor device having a plurality of serially connected logic blocks, an output from a first logic block being coupled to an input of a first latch, the output from the first latch being coupled to the input of a second logic block, an output of the second logic block being coupled to an input of a second latch, the method comprising: detecting a test enable signal; if the test enable signal is active. Mirov, Russell N. et al. (US 5461332 A) teaches an error detection circuit to produce an error signal to halt

operation of the system with which the clock generator system is used, and reset the clock generator. Laird, Douglas et al. (US 5180937 A) teaches delay compensator circuits that compensate for propagation delay variation caused by varying circuit parameters such as supply voltage. Adusumilli, Swaroop (US 6418545 B1) teaches a system and method to reduce scan test pins on an integrated circuit. Jin, London (US 6114892 A) teaches low power consuming scan cells that can be used to perform at-speed testing in scan mode testing with reduced heat dissipation. Sanghani, Amit D. et al. (US 5881218 A) teaches a first clocked flip-flop has a data input latched high, a scan-in input latched high, a clock input coupled to a signal source generating a periodic waveform, a scan-enable input coupled to a scan enable signal, and an output. Narayanan, Sridhar et al. (US 5774474 A) teaches a scan enable signal to scan circuits through a distribution network. Simpson, David L. et al. (US 5347520 A) teaches a boundary-scan enable cell, which includes critical and non-critical enable paths without adding an extra layer of logic. Ozawa, Hidekiyo et al. (US 4491935 A) teaches a means whereby output data is obtained by selecting a constant for determining the number of shift stages of the counter and a scan address in accordance with a scan enable signal, are provided to the operator. Shau, Jeng-Jye (US 6427222 B1) teaches methods to support wafer level testing or wafer level calculations of integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
September 7, 2002

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